MASSACHUSETTS INSTITUTE OF TECHNOLOGY
ARTIFICIAL INTELLIGENCE LABORATORY

Memo No. 323 January 1975

ORIENTING SILICON INTEGRATED CIRCUIT CHIPS FOR LEAD BONDING

by
Berthold K. P. Horn

ABSTRACT

Will computers that see and understand what they see revolutionize industry by automating the part orientation and part inspection processes? There are two obstacles: the expense of computing and our feeble understanding of images. We believe these obstacles are fast ending. To illustrate what can be done we describe a working program that visually determines the position and orientation of silicon chips used in integrated circuits.

Work reported herein was conducted at the Artificial Intelligence Laboratory, a Massachusetts Institute of Technology research program supported in part by the Advanced Research Projects Agency of the Department of Defense and monitored by the Office of Naval Research under Contract number N00014-70-A-0362-0005

ORIENTING SILICON INTEGRATED CIRCUIT CHIPS FOR LEAD BONDING

by

Berthold K. P. Horn

Will computers that see and understand what they see revolutionize industry by automating the part orientation and part inspection processes? Predictions have been made and hedged, yet very little has been done so far. There are two reasons:

* Computing power still costs too much.

* Our understanding of real images is too feeble.

We believe these obstacles are eroding quickly. There is now every indication that difficult operations can be automated soon with dramatic productivity increases. For one thing, powerful computers are available now on single integrated circuit chips. At the same time new ideas have emerged that will enable machines to fill jobs that are too tedious or dangerous to attract human labor. Already one machine in the field is reading hand-written ZIP codes [1]. Another is visually inspecting printed-circuit cards for etching defects at faster than human speed and better than human reliability [2].

To illustrate what can be done, we describe a working program that visually determines the position and orientation of tiny silicon chips, a necessary prerequisite to establishing electrical contact between the chips and the leads protruding from the plastic cases enclosing them. Human operators perform this task for every transistor and integrated circuit made today by peering through a microscope or viewing a TV enlargement.

HOW INTEGRATED CIRCUITS ARE MADE

Figure 1 shows a typical integrated circuit (I.C.) layout and figure 2 illustrates the way it would be connected up inside a dual inline package (D.I.P.). The photographs in figures 3 and 4 show I.C.'s lead-bonded into D.I.P.'s and hybrid circuits. Many individual integrated circuits are fabricated together on a single two- or three-inch wafer as in figure 5. As if it were a sheet of glass, the wafer is scored with a diamond tool and then split up into individual circuits ready for installation in the standard plastic packages. Tiny probe electrodes are applied to each chip in turn to see if it works. Defective chips are marked with an ink spot.

After a chip is bonded to the substrate automatic equipment can attach gold or aluminium wires from pads on the chip to the much larger conductors that extend out of the package. Unfortunately the target pads are not registered precisely with the lines of cleavage and the chips slip a bit as they are laid down, thus losing precise alignment. Consequently the position and orientation of the chip must be determined accurately before the automatic equipment takes over. Typically the human operator moves cross-hairs to the target centers using a joy stick.

Newer techniques limit the problem somewhat by using I.C. chips with reinforced gold-ball contacts as shown in figure 6. These can be bonded directly to either lead-frames, as in figure 7 or film-carriers, as in figure 8. The greater expense of this process is warranted only because it simplifies the manual alignment operation. Since the frame bears a prong for each pad, only one alignment operation is needed for each chip, rather than one for each pad connected to. Still alignment remains the only operation not yet automated. The cost of this is difficult to separate from other steps, but it ranges from perhaps 3 cents for simple chips mass-produced abroad to 30 cents for complicated chips made domestically.

A BORDER SIMPLIFIES PROCESSING

Quick processing of complicated objects usually requires exploitation of special properties that make complete image analysis unnecessary. Sometimes slight redesign helps. In particular, addition of an aluminium border to integrated circuit chips considerably simplifies the orientation task. By happy accident some of the newer Schottky TTL chips now appear with such borders anyway, as seen in figures 9 and 10. Since some chip area is sacrificed, generalizing our method may be desirable when handling chips which do not need borders for other reasons.

THE IMAGE CAN BE PROCESSED QUICKLY BY INEXPENSIVE EQUIPMENT

Figure 11 is a diagram of the system used. All modules are standard items; nothing is exotic. Since the overall system was designed for flexible study of a broad range of applied problems, the sophistication and cost far exceed what is necessary. We estimate that a system costing $15,000 would do the job easily now, with further reduction likely as the cost of mini- and micro-computers continues down. (In fact there is a nice positive feedback loop at work since lead-bonding is a substantial component of the cost of the integrated circuits inside the necessary processing equipment.) In addition, part of the equipment could be shared among a number of work-stations.

Inexpensive or not, no slow technique would be of much interest to industry. It is therefore fortunate that the visual processing can be done in less than .25 seconds. To do so requires some work, however. The mismatch of TV vidicon speed and computer speed is the first problem to face. Since a binary approximation of the image cannot do the job, several bits of analog to digital conversion are needed. But multiple gray level conversion at video speed requires talented and expensive A to D hardware as well as fancy memory buffering.

Picking off and converting one point per horizontal scan is the easy solution. Using this technique, intensities from one vertical line of points can be

collected for each complete set of horizontal scans. The entire image can be acquired by increasing the time between initiation of horizontal scan and sampling, thus stepping the vertical line of sampled points across the image. About 17 seconds are required to record a complete image of 480. by 512. pixels this way. Fortunately, however, the chip orienting program need not look at a complete image. In fact only those points indicated in figure 12 are quite adequate and they are obtainable from four picture frames in .066 second. The four diagonal lines intersect the chip frontiers at eight points. Finding them enables measurements of pad position accurate to .5 mils, given that initial errors are within approximately

$$\Delta x < 15 \text{ mil}, \Delta y < 10 \text{ mil}, \Delta\theta < 25^\circ$$

Initial placement ordinarily falls within these limits. If the chip is further away from the expected position, nothing is lost beyond the time required for an extra pass of the process following coarse adjustment by the first try. There is a trade-off between accuracy and tolerance for large positioning errors, controlled by the placement of the four diagonal scan lines. The positional accuracy of .5 mils is quite satisfactory since the target pads are typically four mils on a side and the connecting wire is one mil in diameter.

THE IMAGE IS NOT BINARY

Surprises await the person that thinks I.C. images are trivial. In fact they are complicated enough to be interesting but not so complicated as to require great sophistication. Under proper uniform lighting conditions, the silicon material itself is relatively dark and the metalization lighter and not very grainy, but transitions between dark and light are not strictly step-like. Figure 13 illustrates the point. The intensity profiles exhibit local irregularities rather than steady change because the edges of I.C. chips are ragged and sloped like those of mesas. Specular reflection points riddle these edges foiling reliance on simple threshholding. To do

the job therefore requires built-in knowledge about edge profile processing. Figure 5 illustrates these important steps:

* Search forward looking for the chip's aluminium border. The first sign is a rapid rise in intensity extending over several pixels.

* Next move further ahead looking for the maximum intensity.

* Search backward to find the minimum.

* Calculate (max + min)/2 and find where the waveform crosses this threshhold. This is the hypothesized edge of the I.C.

The minimum and maximum points tend to be in the midst of plateaus from which they differ only slightly in intensity value. Consequently a small amount of noise somewhere on a plateau can move an extremum considerably. For this reason, averaging between the places where the minimum and maximum are found is not a good way to find the edge. Using the threshhold idea is a standard way to avoid the problem.

Signal noise, dust, and scratches cause occasional miscalculation of an intersection point. This rarely interferes with correct positioning, however, because once the boundary is identified as above, built-in verification steps insure that the result is sound. These include checks on the difference between maximum and minimum, the width of the light and dark plateaus, the width of the transition, and so on, as illustrated by the measurements indicated in figure 14. A failure initiates further profile analysis and if this too fails, the chip is moved a short distance in the best-guess direction and rescanned. Geometrical tests are also performed to ensure that the eight transition points found do indeed lie on a rectangle and that the rectangle has the correct dimensions.

Notice that individual intensity patterns may deviate considerably from the expected shape. Some, for example, may have an abrupt depression in the high intensity plateau caused by a normal gap in the border material. Others have sharp pinnacles where conchoidal fractures cause specular reflections. Template matching schemes are hard pressed by such problems because it is hard to supply them with specific knowledge about particular anomalies. Thankfully, building knowledge into procedures is immensely easier.

Altogether the approach resembles Shirai's treatment of scene analysis in the world of blocks and wedges, long a favorite of workers in artifiicial intelligence [3]. Indeed Shirai's feature point program is a generally important source of ideas with which everyone in image processing should be familiar.

CALIBRATION IS EASY

The program needs the relationship between pixels and the step size of the positioning table. There are several factors which influence this: pixel size varies with each vidicon tube; the pixel size differs in x and y; there is some relative rotation between the camera and the table; and the x and y axes in the camera are not exactly orthogonal. The following linear transformation accounts for these factors:

$$\begin{vmatrix} x_v \\ y_v \end{vmatrix} = \begin{vmatrix} a & b \\ c & d \end{vmatrix} \begin{vmatrix} x_t \\ y_t \end{vmatrix}$$

Where x_v and y_v are pixel units and x_t and y_t are table step units.

Matrix elements a, b, c, and d are easily obtained by observing the displacement in the vidicon which results from stepping a standard I.C. through known calibration points. The inverse matrix then gives correct table movement for observed offsets. Refinement of this calibration process aimed at compensating for non-

linear distortion in the vidicon camera would increase accuracy, although further improvement does not seem necessary at the moment.

AN INDUSTRIAL REVOLUTION IS NEEDED

We believe this application and others like it are the vanguard of a new kind of productivity technology, one oriented toward facing difficult industrial vision and manipulation tasks squarely. Past solutions always involved using people or costly, inflexible special purpose automation. But people are moving increasingly toward the service sector and away from the boredom of the assembly line. Many of the things they do are difficult to automate because special purpose automation costs too much or cannot work. Thus the need for progress in vision-based productivity technology is acute.

Even in the electronics industry, well known for its aggressive posture with respect to new ideas, there are many other examples of expensive, manual assembly, inspection, and repair operations. Here are just a few:

Inspection of Printed Circuit Cards:

When a large circuit board comes out of the etching bath it is likely to have many crack and bridging defects. These must be found and corrected before component insertion. Later on the board must be inspected again after wave soldering, again with many hand corrections necessary. The Japanese have made some progress on this problem [2].

Assembly of Electronic Circuits:

Not all components can be handled by automatic insertion machines. Visual inspection is required in any case. Large or

odd-shaped components such as transformers and components with floppy leads present special problems.

Repair of Assembled Modules:

With larger board areas the yield of working circuits is low. The "new" computer is actually a repaired computer debugged by an expensive, trained technician.

Eventually machine vision is likely to increase productivity in such diverse activities as undersea and underground mining, farming chores, surveillance of dangerous machines, package sorting, custodial care, planetary exploration, and the manufacture of shoes, clothes, and other consumer goods. Everyone knows that these are tough problems to hand over to flexible computer-based systems. Until now the technology has not been adequate and computation costs have not been low enough to move machines with these capabilities out of the laboratory and into the manufacturing process. The great strides that have been made in automating continuous processes like oil refining and paper making, or in discrete parts manufacturing for that matter, have yet to be matched in situations requiring mechanical assembly or human quality visual inspection. It is time to catch up.

ACKNOWLEDGMENTS

Thanks go to Patrick Winston for helping prepare this short note and Karen Prendergast for helping prepare the sketches.

REFERENCES

1. Ken-ichi Mori, Hiroshi Genchi, Sadakazu Watanabe and Sumio Katsuragi, Microprogram Controlled Pattern Processing in a Handwritten Mail Reader-Sorter, Pattern Recognition, Vol 2, 1970, 175-185.

2. Masakazu Ejiri, Takeshi Uno, Michihiro Mese and Sadahiro Ikeda, A Process for Detecting Defects in Complicated Patterns, Computer Graphics and Image Processing, Vol 2, 1973, 326-339.

3. Yoshiaki Shirai, A Context Sensitive Line Finder for Recognition of Polyhedra, Chapter 3, The Psychology of Computer Vision, P. Winston (Ed), McGraw-Hill, 1975.

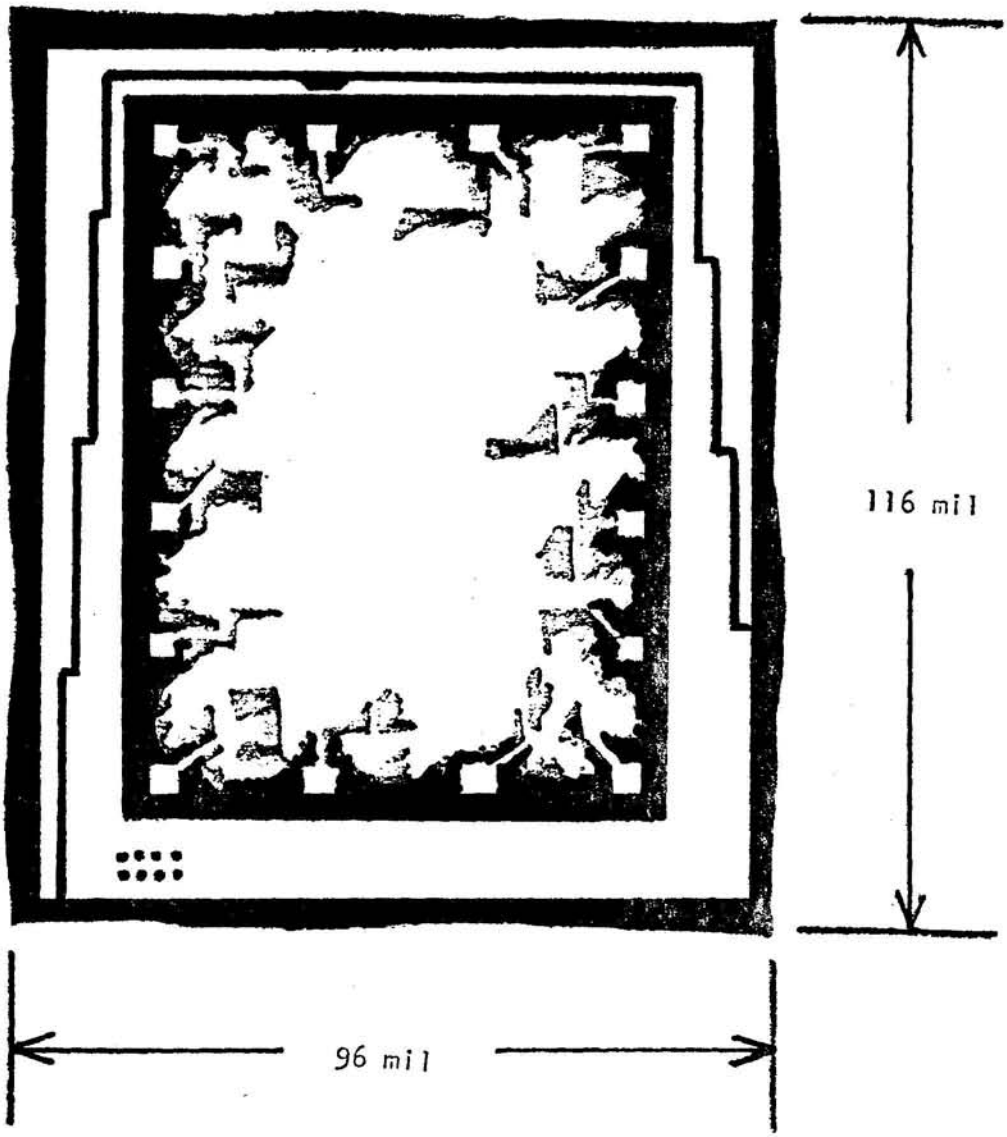

Figure 1: Sketch of integrated circuit silicon chip showing dark silicon edging, bright aluminium border and connecting pads.

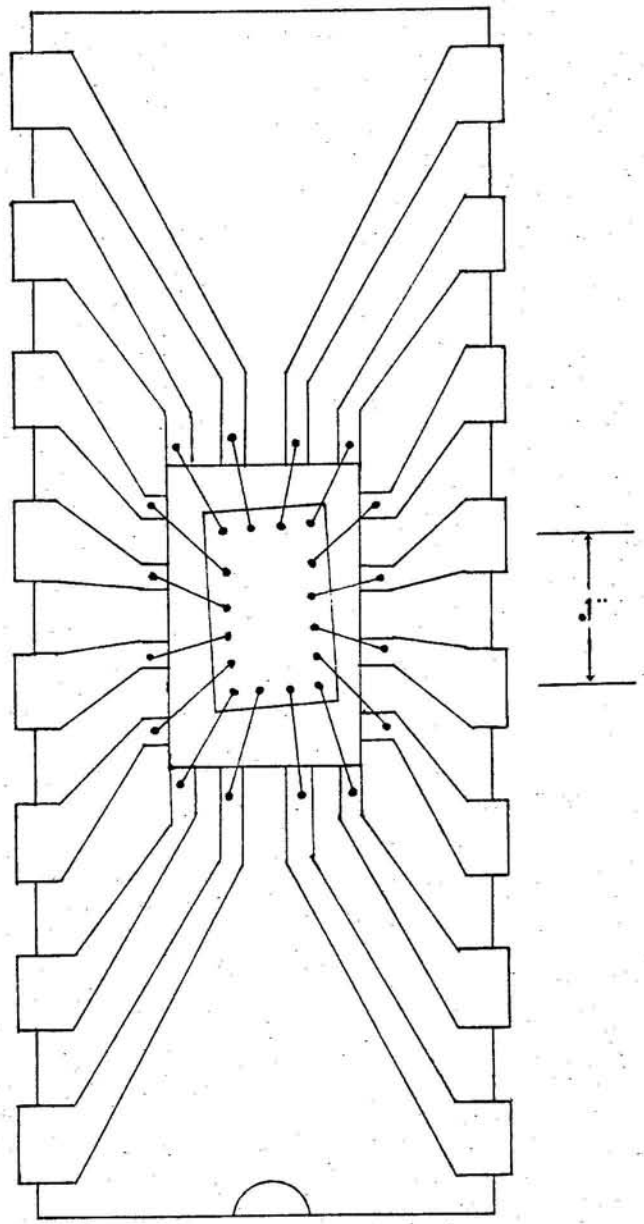

Figure 2: Sketch of typical sixteen-pin dual-inline-package illustrating how the integrated circuit chip is connected to the leads embedded in package.

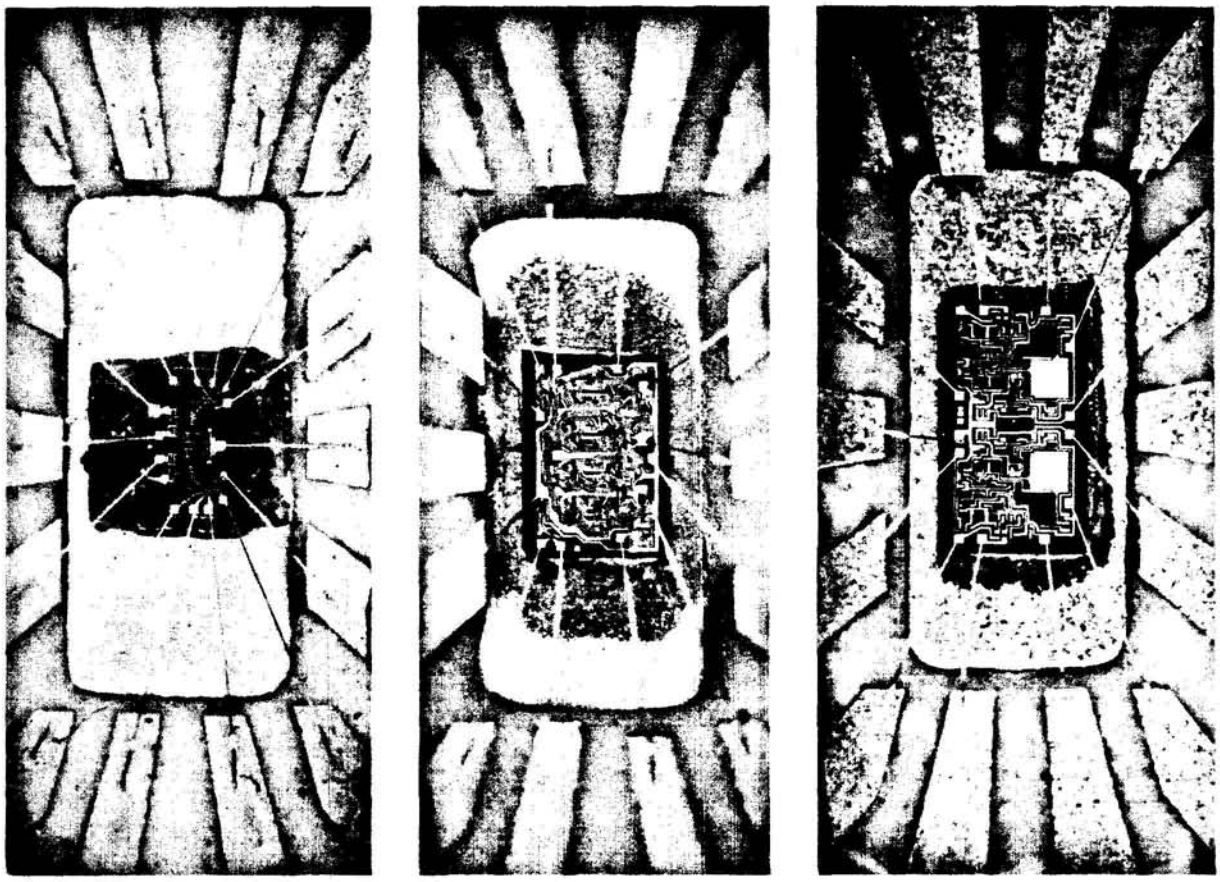

Figure 3: Typical integrated circuit chips lead-bonded into fourteen-pin dual-inline-packages using one-mil aluminium wire.

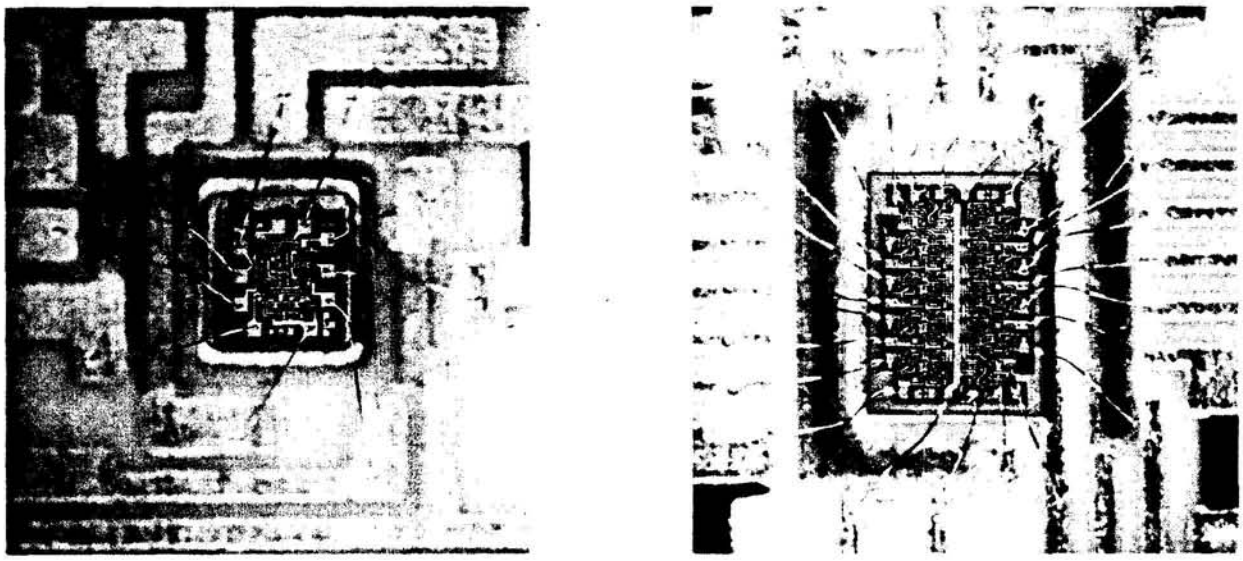

Figure 4: Typical integrated circuit chips lead-bonded into hybrid circuits using one-mil gold wire.

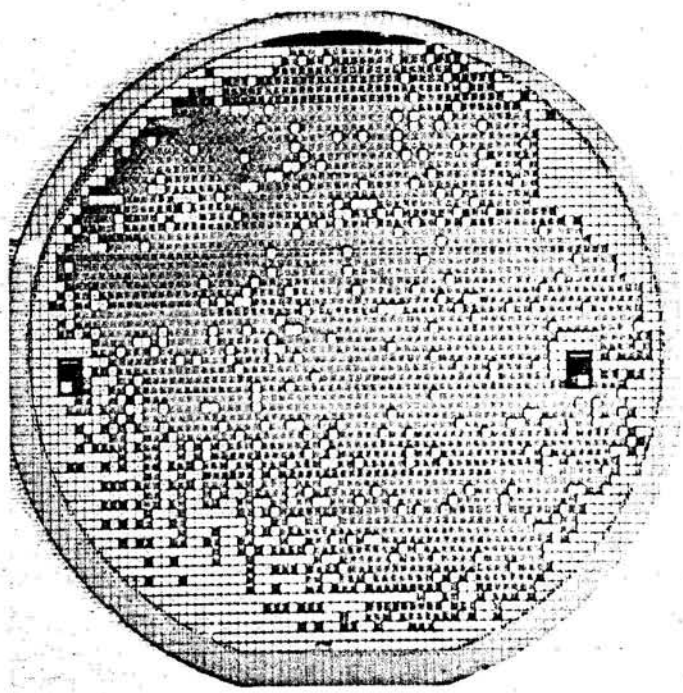

Figure 5: Standard 3" wafer, only defective chips have been left behind.

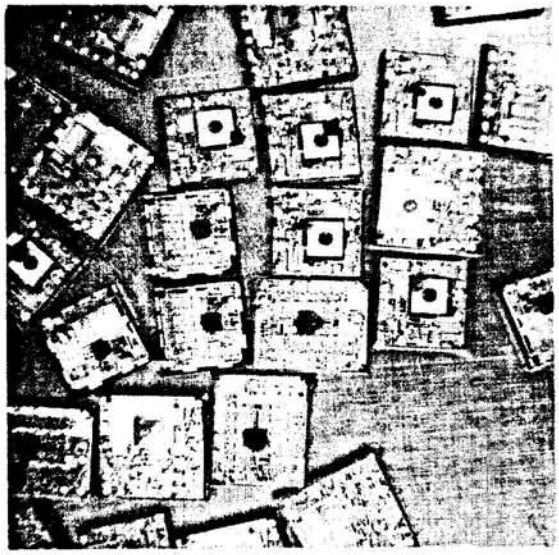

Figure 6: Chips with reinforced pads for lead-frame attachment. (They happen to be defective ones)

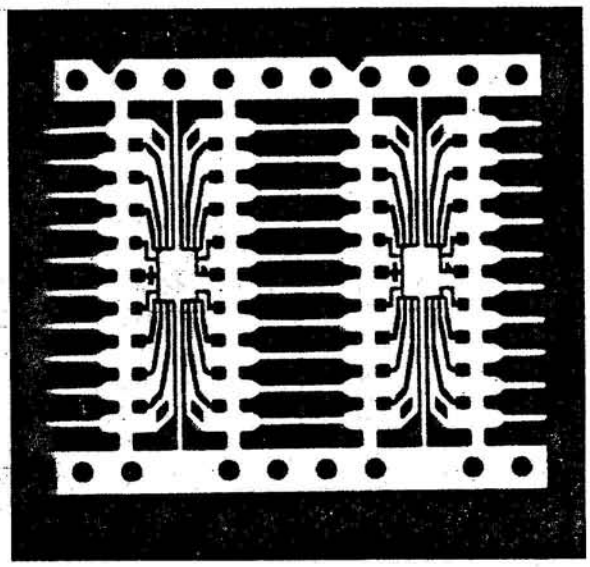

Figure 7: Lead-frame strip of ten-mil gold-plated brass.

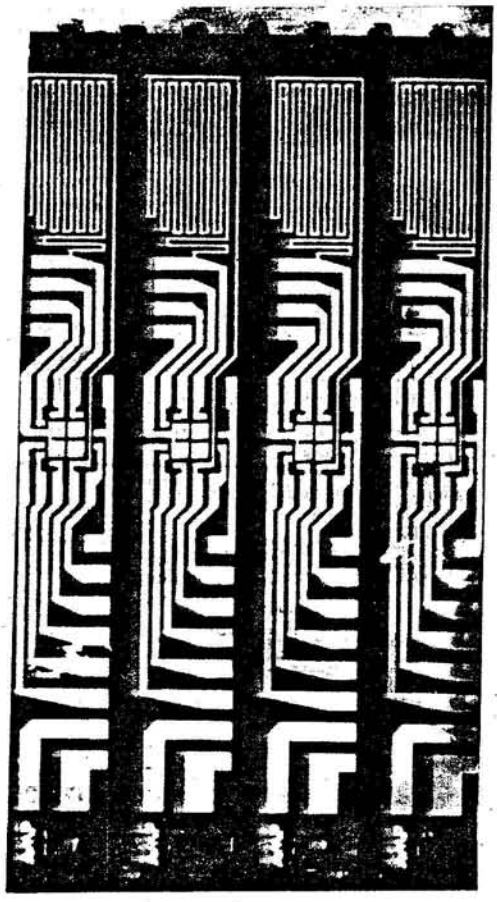

Figure 8: Film-carrier strip.

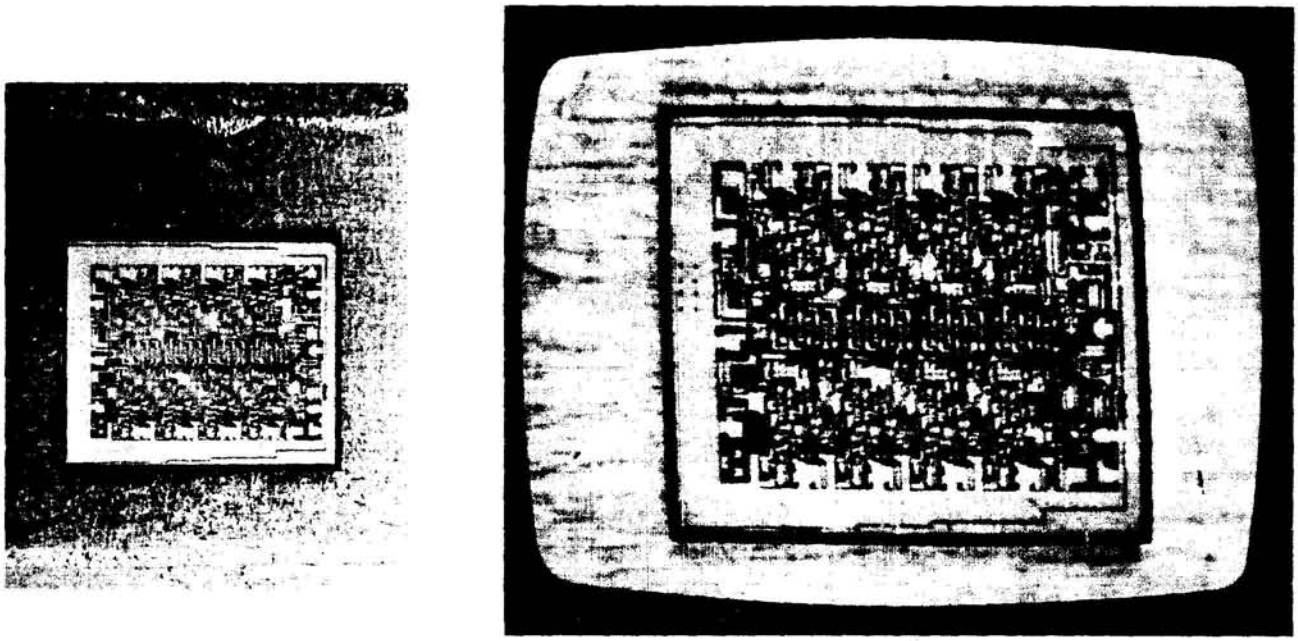

Figure 9: Micrograph and photo of TV monitor image of integrated circuit chip with bright aluminium border. Note dark gap in the border.

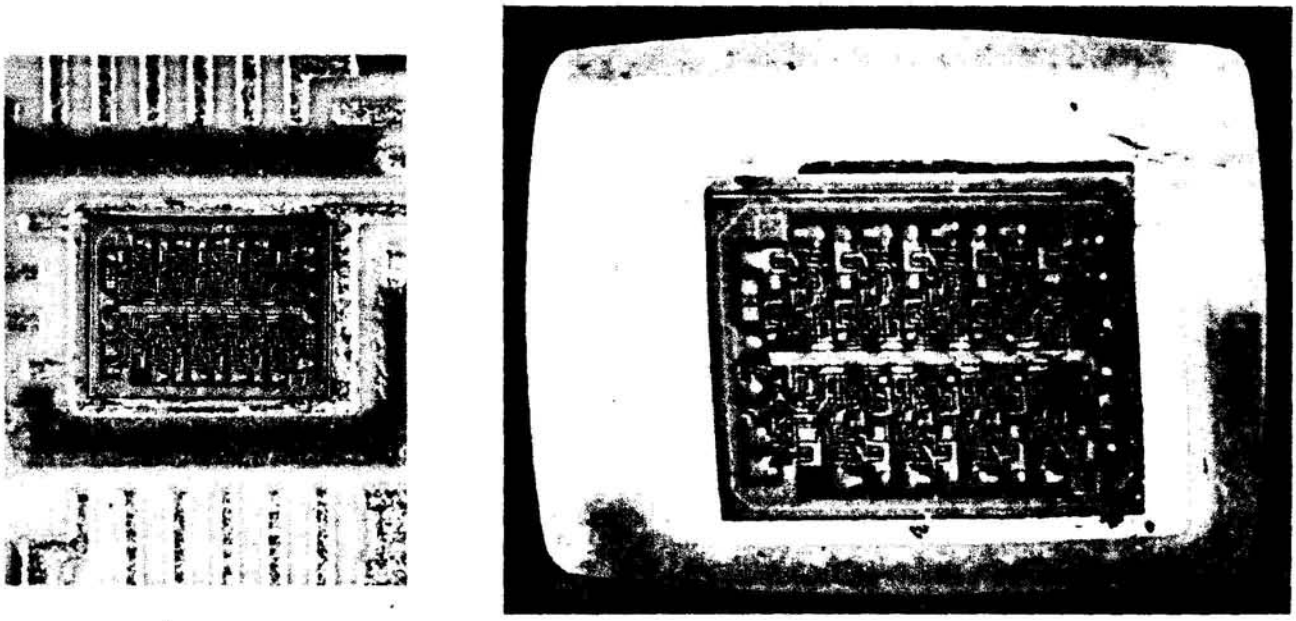

Figure 10: Micrograph and photo of TV monitor image of integrated circuit chip with bright aluminium border. Note high-lights on pads caused by probing electrodes.

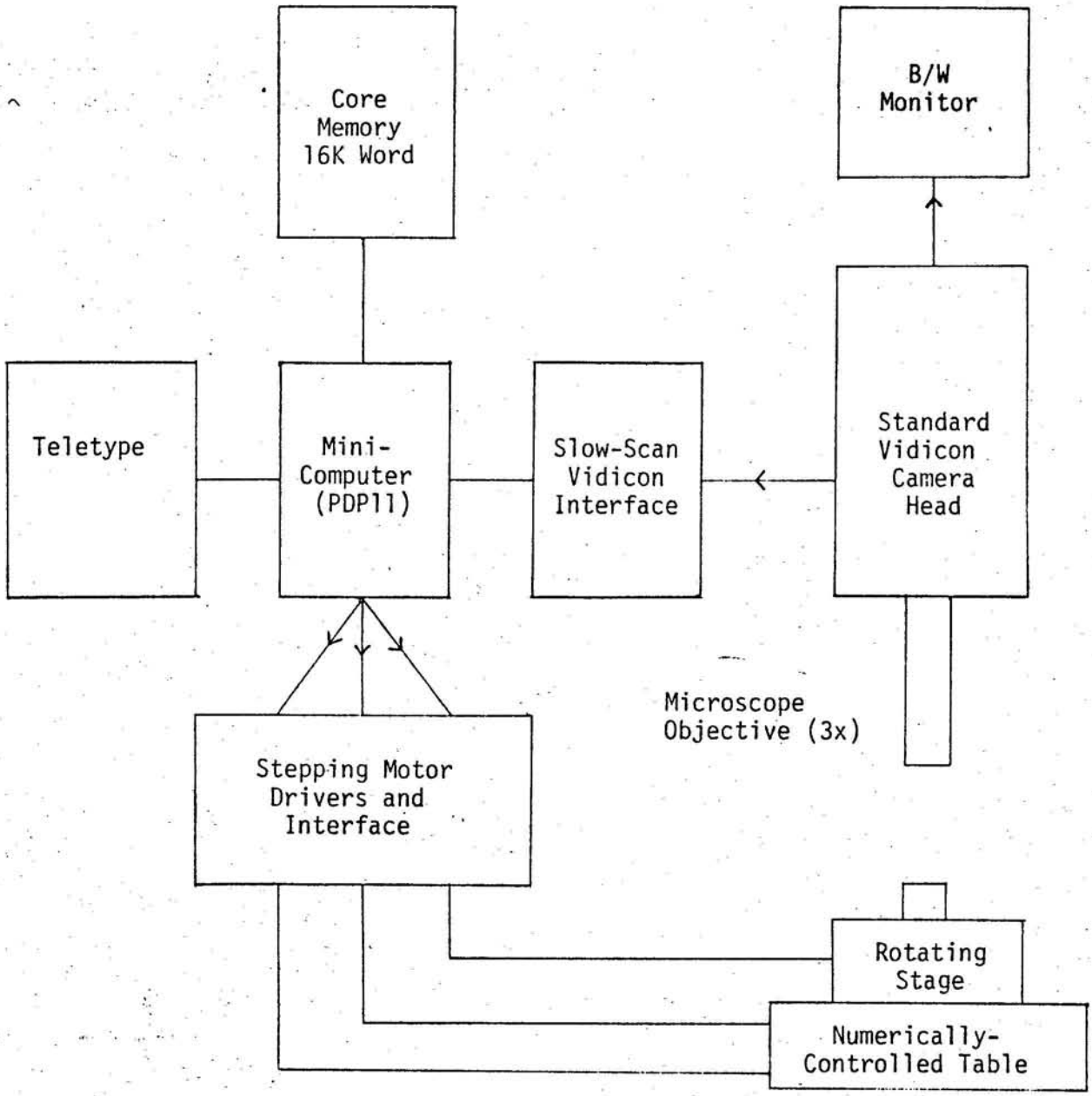

Figure 11: Block-diagram of system used for laboratory demonstration of automatic positioning and orienting of integrated circuit chips using visual input.

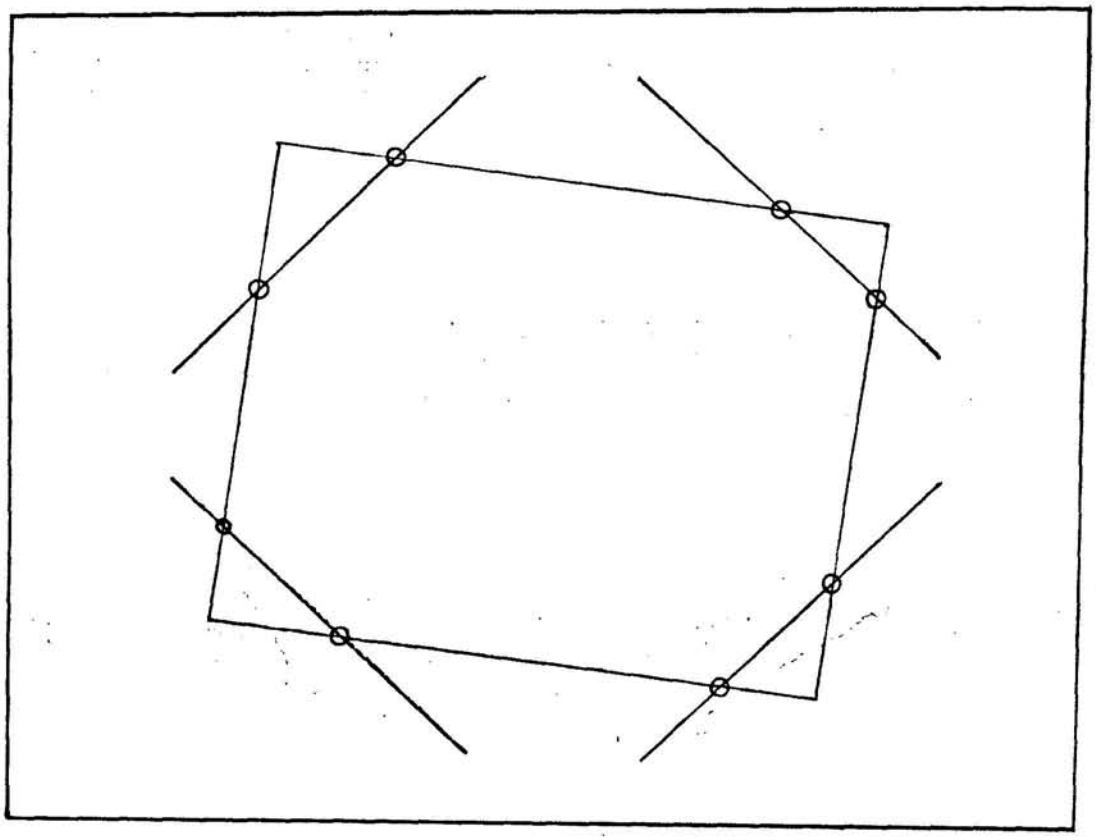

Figure 12: The four diagonal scan lines superimposed on a sketch of the image of an integrated circuit chip. Circles correspond to the eight edge points found by the program.

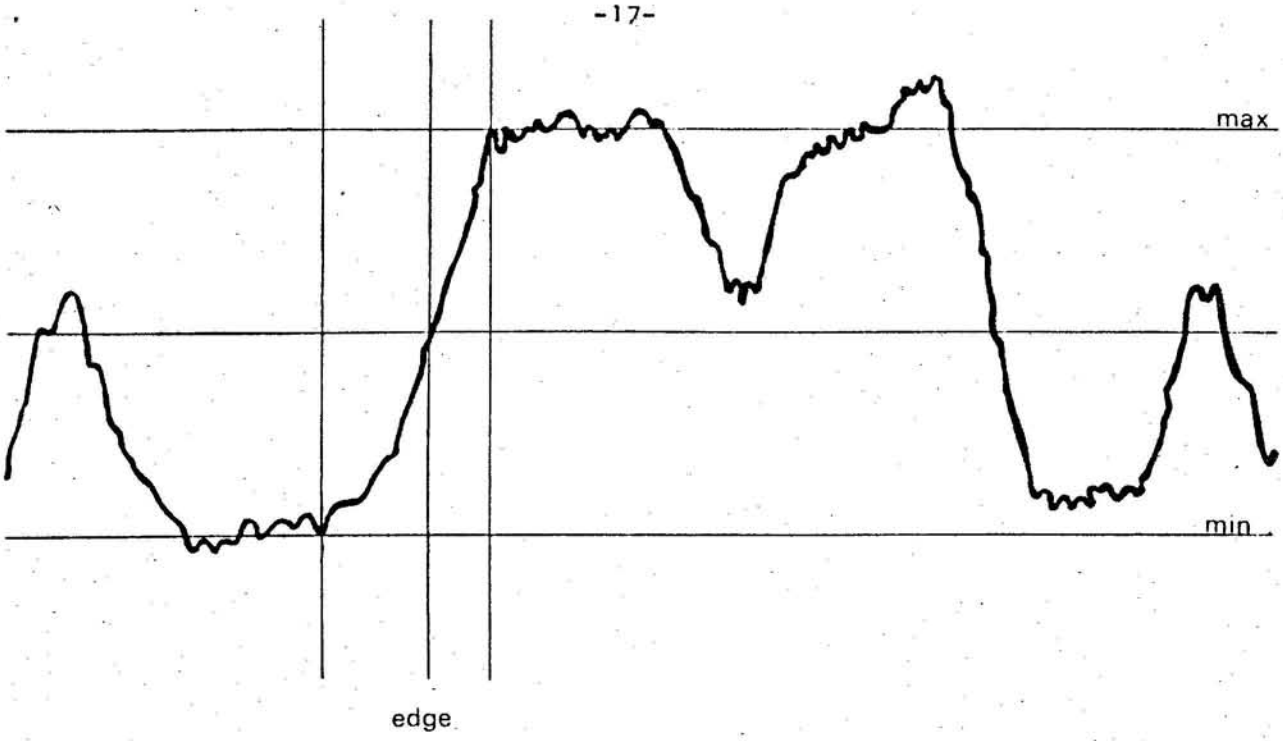

Figure 13: Illustration of the waveform and measurements taken to determine a hypothesized edge position.

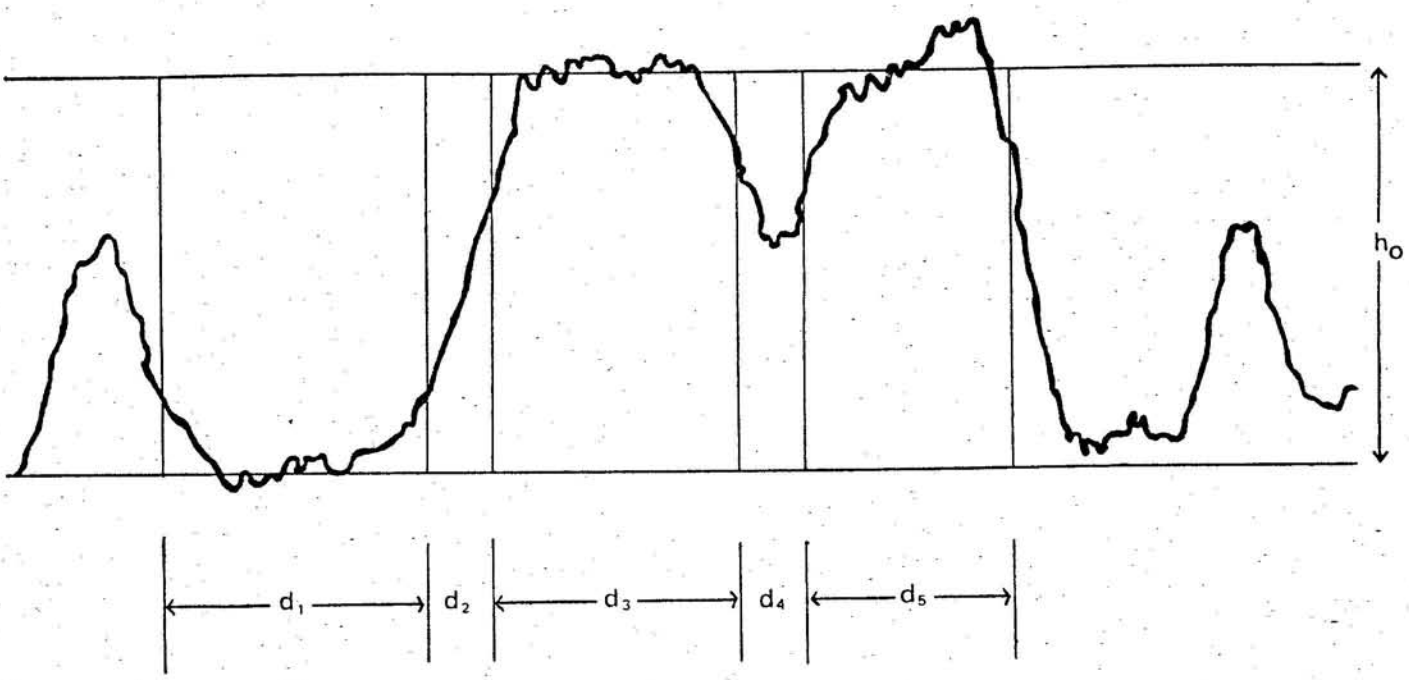

Figure 14: Illustration of the waveform and some of the measurements taken to verify a hypothesized edge position.